region. The surrounded region includes a depletion layer having a composition surface which is in contact with the insulating layer. The MOS transistor comprises an EIB-MOS transistor of which the substrate is adapted to be applied with a voltage of a first polarity for inducing charges of a second polarity over the composition surface of the surrounded region.

IN THE SPECIFICATION:

Kindly replace the paragraph bridging pages 1 and 2, with the following:

Normally, the threshold voltage is approximately constant while the transistor is turned on and off, however, it is possible to control the threshold voltage by changing a substrate voltage of the MOS transistor. That is, the threshold voltage shift ΔV_{th} is expressed according to the following equation.

$$\Delta V_{th} = -\gamma V_{bs} \qquad (1)$$

wherein γ is a body effect factor of the MOS transistor. Therefore, one way to compromise the fast operation and the reduction of the power consumption of the MOS transistor is that the threshold voltage is lowered when the MOS transistor is turned on and rises when the MOS transistor is turned off by changing the substrate voltage of the MOS transistor.

Kindly replace the paragraph beginning at page 2, line 6, with the following:

In case of a VTMOS transistor composed by using the VTMOS technique, the threshold voltage of the VTMOS transistor is controlled by a whole of a chip in which the VTMOS transistor is provided. In this case, a first voltage is applied to a substrate of the VTMOS transistor in the active mode, and a second voltage smaller than the first voltage is applied to the substrate in the standby mode, thereby, the threshold voltage rises.

Kindly replace the paragraph beginning at page 2, line 12, with the following:

On the other hand, a DTMOS transistor such as a n type DTMOS transistor shown in Fig. 1 composed by using the DTMOS technique comprises a SOI 4 which includes a substrate 1 composed of a p type semiconducting material (e.g. silicon), a single crystal layer 2 composed of a semiconducting material (e.g. silicon) and an insulating layer 3 (e.g. silicon dioxide layer) interposed between the substrate 1 and the single crystal layer 2. The single crystal layer 2 is formed therein with a n type source region 5, a n type drain region 6 and a p type body 7 surrounded by the source region 5 and the drain region 6. Further, a gate electrode 9 deposited on the body 7 through a gate oxide 8 is electrically connected to the body 7 through a wire 10 so that the threshold voltage of the DTMOS transistor is controlled. In other words, the threshold voltage is always lowered when the DTMOS transistor is turned on, and it always rises when it is turned off.

Kindly replace the paragraph beginning at page 3, line 11, with the following:

With reference to the equation (1), in order to control the threshold voltage effectively, it is preferable to make the body effect factor γ high. However, in general, it is necessary to raise an impurity concentration of the MOS transistor in order to make the body effect factor of the MOS transistor high. As a result, the threshold voltage itself rises, and the fast operation of the MOS transistor is degraded. In such a circumstance, an optimization of the body effect factor γ has not been performed so far, and the body effect factor γ is normally about 0. 1 to 0. 3.

Kindly replace the paragraph bridging pages 3 and 4, with the following:

Wherein t_{fox1} is a thickness of a gate oxide 15 interposed between the substrate 13 and a gate electrode 14, and 1_d is a depth of a depletion layer formed directly below the gate oxide 15. Therefore, it is necessary to raise the impurity concentration and lower the depth 1_d in order to make the body effect factors γ high. However, the threshold voltage becomes high if the impurity concentration becomes high, as described. This situation holds true in case of a partially depleted SOI MOS transistor.

IN THE CLAIMS:

Please add new claims 7-12 as follows.

--7. (New) A MOS transistor with a threshold voltage controlled by changing a body potential of the MOS transistor, comprising: